

What is claimed is:

1. An apparatus for sharing a resource between at least two components, comprising:
 - a resource having a plurality of elements;
 - an access controller coupled to said resource; and
 - at least first and second components coupled to said access controller and adapted to access the elements of said resource, wherein said access controller is adapted to control which of said components are able to access which elements of said resource.
2. An apparatus for sharing a resource, comprising:
 - a resource having a plurality of elements;
 - an access controller coupled to said resource;
 - at least first and second components coupled to said access controller and adapted to access the elements of said resource; and
 - an access controller adapted to store a first mask value, wherein access to the elements of said resource is controlled based on said first mask value.
3. The apparatus of claim 2 wherein said first mask value represents which of the elements of said resource are available for access for a selected component.
4. An apparatus for partitioning a memory resource, comprising:
 - a memory resource having a plurality of addressable blocks;

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first and second components adapted to access said memory resource; and
a register adapted to store a first mask value, wherein access to addressable blocks of said
memory resource is controlled based on said first mask value.

5. The apparatus of claim 4 wherein said memory resource is a cache memory.
6. The apparatus of claim 5 further comprising:
a processor coupled to said cache memory, wherein said first component includes
execution of instructions by said processor from a first thread and said second component
includes execution of instructions by said processor from a second thread.
7. The apparatus of claim 6 wherein said first mask value represents which of the
addressable blocks of said cache memory are available for eviction.
8. The apparatus of claim 7 wherein a first mask value is provided for each of said
components, said first mask values indicate which of the addressable blocks of said cache
memory are available for eviction for one of said components and which of the addressable
blocks of said cache memory are available for eviction for at least two of said components.
9. The apparatus of claim 8 wherein an eviction array is provided indicating the least
recently used addressable block of said cache memory and a second mask is provided, said

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second mask value selecting which bits of said eviction array are used in controlling which of the addressable blocks of said cache memory are available for eviction.

10. The apparatus of claim 6 wherein an eviction array is provided indicating the least recently used addressable block of said cache memory and wherein said first mask value is an auxiliary mask value and said auxiliary mask value represents which of the addressable blocks of said cache memory are available for eviction and selects which bits of said eviction array are used in controlling which of the addressable blocks of said cache memory are available for eviction.

11. A method for sharing a resource having a plurality of elements between at least first and second components, comprising:

controlling, with an access controller coupled to said at least first and second components, which of said at least first and second components are able to access which elements of said resource.

12. The method of claim 11 further comprising:

storing a first mask value, wherein access to the element of said resource is controlled based on said first mask value.

13. The method of claim 12 further comprising:

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determining which of said first and second components is accessing said resource; and
determining which of the elements of the resource are available for access by the
component accessing said resource based on said first mask value.

14. The method of claim 13 further comprising:

providing an eviction array indicating the least recently used element of said resource;
providing a second mask value; and
selecting which bits of said eviction array are used in controlling which of the elements of
said cache memory are available for access by the component accessing said resource based on
said second mask value.

15. The method of claim 14 further comprising:

determining which element of the resource can be accessed by the component accessing
said resource.

16. The method of claim 12 wherein said first mask value is an auxiliary mask value, the
method further comprising:

determining which of said first and second components is accessing said resource;
providing an eviction array indicating the least recently used element of said resource;
determining which of the elements of the resource are available for access by the
component accessing said resource based on said auxiliary mask value; and

selecting which bits of said eviction array are used in controlling which of the elements of said resource are available for access by the component accessing said resource based on said auxiliary mask value.

17. The method of claim 16 further comprising:

determining which element of the resource can be accessed by the component accessing said resource.

18. A set of instructions residing in a storage medium, said set of instructions capable of being executed by a processor for sharing a resource having a plurality of elements between at least first and second components comprising the steps of:

controlling, with an access controller coupled to said at least first and second components, which of said at least first and second components are able to access which elements of said resource.

19. The set of instructions of claim 18, wherein the execution of said set of instructions further comprises the step of:

storing a first mask value, wherein access to the element of said resource is controlled based on said first mask value.

20. The set of instructions of claim 19, wherein the execution of said set of instructions

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further comprises the steps of:

determining which of said first and second components is accessing said resource; and

determining which of the elements of the resource are available for access by the component accessing said resource based on said first mask value.

21. The set of instructions of claim 20, wherein the execution of said set of instructions

further comprises the steps of:

providing an eviction array indicating the least recently used element of said resource;

providing a second mask value; and

selecting which bits of said eviction array are used in controlling which of the elements of said cache memory are available for access by the component accessing said resource based on said second mask value.

22. The set of instructions of claim 21, wherein the execution of said set of instructions

further comprises the step of:

determining which element of the resource can be accessed by the component accessing said resource.

23. The set of instructions of claim 19, wherein said first mask value is an auxiliary mask

value and wherein the execution of said set of instructions further comprises the steps of:

determining which of said first and second components is accessing said resource;

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providing an eviction array indicating the least recently used element of said resource;
determining which of the elements of the resource are available for access by the component accessing said resource based on said auxiliary mask value; and
selecting which bits of said eviction array are used in controlling which of the elements of said resource are available for access by the component accessing said resource based on said auxiliary mask value.

24. The set of instructions of claim 23, wherein the execution of said set of instructions further comprises the step of:

determining which element of the resource can be accessed by the component accessing said resource.

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